

SF20AG - SF20JG

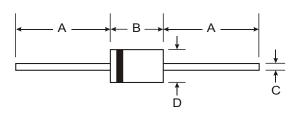
2.0A SUPER-FAST GLASS PASSIVATED RECTIFIER

Features

- Glass Passivated Die Construction
- Diffused Junction
- Super-Fast Switching for High Efficiency
- High Current Capability and Low Forward Voltage Drop
- Surge Overload Rating to 60A Peak
- Low Reverse Leakage Current
- Plastic Material: UL Flammability Classification Rating 94V-0

Mechanical Data

- Case: Molded Plastic
- Terminals: Plated Leads Solderable per MIL-STD-202, Method 208
- Polarity: Cathode Band
- Marking: Type Number
- Weight: 0.35 grams (approx.)
- Mounting Position: Any



DO-15							
Dim	Min	Мах					
Α	25.40	_					
В	5.50	7.62					
С	0.686	0.889					
D	2.60	3.6					
All Dimensions in mm							

Maximum Ratings and Electrical Characteristics @ T_A = 25°C unless otherwise specified

Single phase, half wave, 60Hz, resistive or inductive load. For capacitive load, derate current by 20%.

Characteristic		Symbol	SF20 AG	SF20 BG	SF20 CG	SF20 DG	SF20 FG	SF20 GG	SF20 HG	SF20 JG	Unit
Peak Repetitive Reverse Voltage Working Peak Reverse Voltage DC Blocking Voltage		V _{RRM} V _{RWM} VR	50	100	150	200	300	400	500	600	V
RMS Reverse Voltage		V _{R(RMS)}	35	70	105	140	210	280	350	420	V
Average Rectified Output Current (Note 1)	@ $T_A = 75^{\circ}C$	Ι _Ο	2.0							А	
Non-Repetitive Peak Forward Surge Current 8.3ms Single half sine-wave Superimposed on Rated Load (JEDEC Method)		I _{FSM}	60								А
Forward Voltage	@ I _F = 2.0A	V _{FM}	0.95 1.3 1.				.5	V			
	@ T _A = 25°C @ T _A = 100°C	I _{RM}	I _{RM} 10 100							μA	
Reverse Recovery Time (Note 2)		t _{rr}	35			40		50		ns	
Typical Junction Capacitance (Note 3)		Cj	75 50							pF	
Typical Thermal Resistance Junction to Ambient		R _{0JA}	40								K/W
Operating and Storage Temperature Range		Tj, TSTG	-65 to +150								°C

Notes: 1. Valid provided that leads are kept at ambient temperature at a distance of 9.5mm from the case.

- 2. Measured with $I_F = 0.5A$, $I_R = 1.0A$, $I_{rr} = 0.25A$. See Figure 5.
- 3. Measured at 1.0MHz and applied reverse voltage of 4.0V DC.



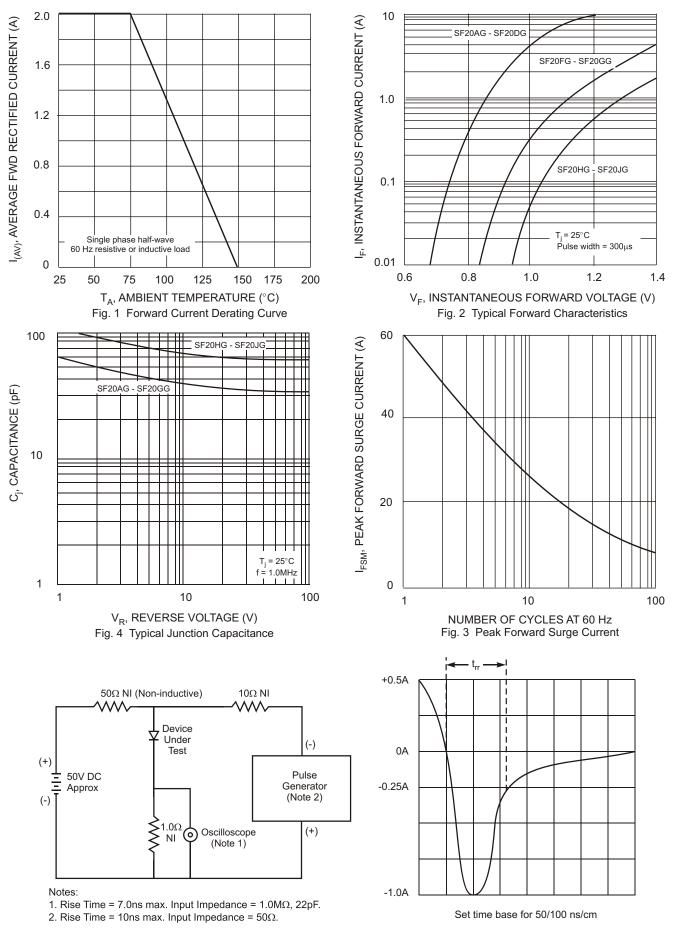


Fig. 5 Reverse Recovery Time Characteristic and Test Circuit